PATENT SPECIFICATION (11) 1 288 564

DRAWINGS ATTACHED

1 288 564

(21) Application No. 4296/69 (22) Filed 24 Jan. 1969
(23) Complete Specification filed 27 Jan. 1970
(45) Complete Specification published 13 Sept. 1972
(51) International Classification H01L 1/14
(52) Index at acceptance
H1K 211 217 277 306 312 351 352 353 356 36Y 422 42X 441 453 455 459 464 469 470 483 489 511 520 525 52Y 530 532 534 53X 53Y 54Y 55Y 581 60Y 611 615 616 618 61Y 650

(72) Inventor PETER FRANK CASTLE

(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR CHIPS

(71) We, NATIONAL RESEARCH DEVELOPMENT CORPORATION, a British Corporation, established by Statute, of Kingsgate House, 66-74 Victoria Street, London SW1E 6SL, England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a semiconductor device and a process of making it. This invention also relates to a method of mounting a semiconductor device, for example a transistor chip, to a thick or thin film electrical circuit and to the resulting assembly.

Previously, transistors, in conventional manufacture, have been made by placing the semiconductor chip in an encapsulation well known in the transistor technology, or in micro-packages usually made of ceramics, glass or plastics. In all of these known structures, contacts are made internally between the chip and the external leads. The connections to the semiconductor chip are usually made by means of fine wires using thermocompression bonding or ultrasonic bonding techniques, which are both known in the transistor technology. These devices are incorporated in a circuit by attaching the external leads to conductors in the circuit by soldering or welding processes. Thus, the final device is many times larger than the original semiconductor chip, and when fixed into a film circuit occupies a larger area than would the chip on its own. Furthermore, it adds appreciably to the thickness of the circuit assembly. Also with this type of device, the package (also known as the "housing") is expensive and an expensive process is involved in fitting and connecting the chip into the housing. It is also seen that for each terminal, two separate bonds have to be effected and this is reflected in a high cost of manufacture; furthermore, the large number of bonds required increases the possibility of failure.

The present invention provides a silicon semiconductor device with diffused impurities therein forming diffused regions and provided with an apertured insulating film comprising a layer of silicon dioxide, which device is characterized by a metallic contact structure adapted to enable said device to be directly mounted on and electrically connected to a thick or thin film electrical circuit, said contact structure comprising a plurality of electrically conductive pips projecting from that surface of the device in which the diffused regions are situate and each of which is electrically linked with an associated diffused region through electrically conductive material in the apertures in the insulating film via an electrically conductive film composed of a chromium layer which is firmly adherent to said insulating film merging into a gold layer, said conductive pips being (i) of a height which is sufficient to provide clearance between the surface of the device on which they are situate and the circuit when the device is electrically connected and mounted thereon and (ii) composed of a material or combination of materials adapted to be electrically connected to a thick or thin film electrical conductor element by solder flow or ultrasonic or thermocompression bonding techniques, said chromium layer having sufficient electrical conductivity to carry electric current to allow the formation of said pips by electroplating and said gold layer having an electrical conductivity sufficient to carry an operating current for which the device is designed. Said chromium layer may suitably be, e.g., of a thickness of from 50 mμm to 400 mμm, preferably 100 mμm to 200 mμm and said gold layer, e.g., of a

thickness of from 300 mμm to 2 μm. Chromium has excellent adhesion to silicon dioxide and to silicon nitride.

It is to be noted that the electrically conductive material in the apertures of the insulating film may be of chromium but could be, e.g., molybdenum.

The gold and chromium layers may be sintered so as to produce the "merging", the device being heated at between 200°C and 300°C.

A suitable height for the conductive pips may be, for example, at least 10 μm, preferably at least 25 μm. Suitably the conductive pips may be of silver and this may be coated with a layer of tin.

The present invention also provides a process for the production of a silicon semiconductor device with diffused impurities therein forming diffused regions and having (a) an insulating film comprising a layer of silicon dioxide having apertures therein containing electrically conductive material in electrical contact with the diffused regions, and (b), firmly adhering to said insulating film, an electrically conductive film of a chromium layer merging into a gold layer, the chromium layer being nearest to the insulating film, having good adhesion thereto and having sufficient electrical conductivity to allow electroplating by current passing through it, the gold layer having an electrical conductivity sufficient to carry an operating current for which the device is designed, which process comprises

(i) selectively etching away part of said gold layer to expose the underlying chromium layer and to leave a pattern in said gold layer to provide electrical conductors extending from the electrically conductive material in contact with said diffused regions to areas where contact pips are to be produced,

(ii) coating the face of the device having the electrically conductive film thereon with a photoresist material and removing part of it to expose said areas,

(iii) masking the face opposite to that mentioned at (ii) against an electroplating solution,

(iv) electroplating metallic contact pips on said areas to a height which is sufficient to provide clearance between the surface of the device on which they are situate and the surface of a thick or thin film electrical conductor element when the device is electrically connected and mounted thereon, said pips being composed of a material or combination of materials adapted to be electrically connected to said element by solder flow or ultrasonic or thermocompression bonding techniques, the electroplating of the metallic contact pips being effected by using said chromium layer to carry the electroplating current to the areas where the pips are to be produced, and

(v) removing the remainder of said photoresist layer and etching away the exposed regions of said chromium layer using a selective etchant which does not attack either said gold layer or the contact pips.

The electrically conductive pips may be made of, for example, silver, copper, lead, gold or nickel; which metal is chosen for making these pips depends on the technique used to mount the device. When solder flow techniques are used, the pips may be coated with a solder or electroplated with a metal having a melting point below that of the pips and preferably below 300°C. Tin is a preferred metal which may conveniently be electroplated on the pips and is especially suitable for use with silver pips. When the device is placed in contact with thick or thin film conductive circuit elements and heat is applied, the solder, or electroplated metal such as tin, flows and wets and in some cases alloys with the pips and the circuit elements; thus, after the source of heat has been removed, the device becomes bonded and electrically connected to the circuit.

Alternatively, if the thick or thin film circuit elements are themselves coated with solder, it is unnecessary to coat the pips on the device with solder or electroplate with a metal such as tin, the application of heat causing the solder on the circuit elements to flow and wet the pips on the device which, after the heat source is removed, becomes securely connected to the circuit elements.

Gold is an example of a metal which may be used for the pips if thermocompression bonding techniques, well known in the art, are to be used to connect the device to a circuit.

When ultrasonic bonding techniques, well known in the art, are required to be used for connecting the device to a circuit, pips comprising metals such as, for example, silver may be satisfactorily used on the device.

The present invention also provides a method of mounting a semiconductor device of the invention to a thick or thin film electrical circuit, which comprises the steps of positioning the semiconductor device with each conductive pip adjacent to a selected point on the electrical circuit path of the thick or thin film circuit and by solder flow or ultrasonic bonding or thermocompression bonding technique, or combinations of these, causing each conductive pip to become directly electrically connected to the circuit path to which

it is adjacent, so as to form a secure electrical connection between the raised conductive pip and said circuit path, the solder flow or ultrasonic or thermocompression bonding being carried out in such a way that the semiconductor device remains spaced from the thick or thin film circuit after the completion of these operations.

The semiconductor device of the invention may comprise a plurality of diffused structures, some of the pips being common to more than one of these structures.

The semiconductor device of the invention may be provided with one or more dummy contact pips of similar construction to the contact pips proper and of similar dimensions. The dummy contact pips are bonded to the film circuit in the same way as the contact pips proper. Although these dummy contact pips have no electrical connecting function, they serve to improve the stability of the mechanical connection between the semiconductor chip and the film circuit.

The present invention makes it possible to dispense with encapsulation of the semiconductor device and no connections between fine wires and the electrodes of the semiconductor device are required. The dimensions of a mounted chip transistor as specifically described below are therefore small and are thus compatible with the miniature circuit arrangement in which it is included; the mounted chip may, for example, measure only 750 μm by 750 μm and add only 250 μm in height to the assembly.

For a better understanding of the invention reference will now be made by way of example to the accompanying drawings in which:

FIGURES 1A, 2A, 3A, 4A, 5A, 6A and 7A show the stages of processing of one embodiment of the device of the invention sectioned along C - D as indicated in Figure 8 which shows a plan view of the finished product.

FIGURES 1B, 2B, 3B, 4B, 5B, 6B and 7B show the stages of processing of the device sectioned along A - B as indicated in Figure 8.

FIGURE 1C shows a plan view of a transistor with a layer of gold covering all of its upper surface (a layer of chromium being underneath). The dotted regions indicate where contact pips will subsequently be electroplated.

FIGURE 3C shows a plan view of the device with a gold conductor pattern covered by a thin film of photoresist.

FIGURE 9 is a schematic elevational view of the device mounted on a circuit.

Referring to Figures 7A, 7B and 8, a silicon chip 1 has a diffused transistor chip structure 2 (see Figure 7), either NPN or PNP, comprising a base region 17, an emitter region 18 and a diffused collector contact region 10; these diffused regions are produced in known manner by diffusing impurities such as phosphorus and boron into a silicon wafer. The top face of the chip is protected by an insulating film 3 of silicon dioxide or silicon dioxide overlaid with silicon nitride. Three raised contact pips 4, 5 and 6 are produced as described below at the positions indicated on the upper surface of the chip and it is by means of these pips that the chip is eventually connected to a circuit. Contact pips 4, 5 and 6 are electrically connected respectively to the emitter 18, base 17 and collector contact 10 regions of the diffused transistor by means of gold conductors 7, 8 and 9 respectively. A film of chromium 13, underlying conductor patterns 7, 8 aand 9 provides good adhesion of the conductors 7, 8 and 9 to the insulating film 3. Ohmic contact to the diffused regions is provided by an aluminium layer 16.

In this embodiment, the contact pips 4, 5 and 6 are produced as described below; the device may then be mounted on a circuit by solder flow techniques. The pips comprise silver 11 coated with tin 12, each pip being approximately 150 μm in diameter and 37 μm high.

The device may be fitted to a thick or thin film circuit by inverting it and positioning it so that each contact pip is lying over the appropriate conductor pattern. With the application of heat, the tin 12 on the pips melts, forming an alloy with a small amount of silver at the interface of the two metals and also wets the conductors of the circuit. On removing the source of heat, the device becomes securely connected to the circuit. The silver portion of the pip deforms to a negligible extent during the mounting operation and maintains the desired clearance between the device and circuit. A mounted device is shown in elevation in Figure 9 in which the film circuit is referenced 15 and the conductor patterns 14.

When mounted, the device occupies a volume only slightly larger than the chip of silicon which in conventional technology is itself normally mounted inside a very much larger package. Furthermore, expensive and delicate wire bonding operations are avoided.

The method of manufacture of the transistors is as follows, being described with reference to the drawings. In the drawings a single transistor chip is shown for convenience. In practice, the process to be described is carried out on a slice of silicon containing several hundred transistor structures side by side (i.e. an array of tran-

sistor chips) and at the completion of the processing, the slice is cut up by well known techniques to produce the individual transistor chips.

Referring to Figs. 1C, 1A and 1B, showing a single transistor chip, a silicon slice 1 comprises diffused regions (e.g. of phosphorus and boron); the diffused regions for a single transistor chip consist of a collector contact region 10, a base region 17 and an emitter region 18. On the upper surface of the slice 1 there is an insulating film 3 of silicon dioxide; the insulating film contains three openings in positions such that portions of the diffused regions 10, 17 and 18 are exposed; a layer of aluminium 16 of thickness about 300mμm fills each of these three openings in the insulating film 3, said layer having been sintered in known manner to form low resistance electrical contacts with each of the diffused regions. A film of chromium 13 of a thickness of about 150mμm and a film of gold 19 approximately 1μm thick cover the upper surface of the slice 1 in such a way that good electrical contact is made with the three diffused regions through the aluminium layers. The procedures for applying the chromium and gold films are well known ones in the technique of making silicon semiconductor devices of this kind.

The techniques utilised to produce the contact structure on the device are as follows:

1) A film 20 of a photoresist material e.g. AZ-111 produced by Shipley Chemicals Ltd. is applied over the upper surface of the gold film (see Figs. 2A and 2B). Using a suitable mask, the photoresist is exposed to ultraviolet radiation and then developed to leave regions 7, 8 and 9 of the gold film 19 coated with photoresist 20 (see Figs. 3A, 3B and 3C). In Fig. 3C, the regions 7, 8 and 9 of the gold film coated with photoresist 20 are denoted by reference numerals 20/7, 20/8 and 20/9 respectively. The exposed gold is then removed using a selective etchant, e.g. a solution of iodine and potassium iodide, which does not attack the chromium film 13 and therefore leaves this covering the whole slice. The remaining photoresist is then removed using a commercially available stripper appropriate to the photoresist, leaving the pattern of gold conductors 7, 8 and 9 on top of the chromium film 13 (see Figs. 4A and 4B).

2) The upper surface of the slice is then coated with another film, 21, of photoresist, e.g. Kodak Thin Film Resist (i.e. KTFR) manufactured by Eastman Kodak Company, Rochester, New York, USA, which is processed (i.e. masked, exposed to ultraviolet radiation and developed) to provide circular openings 22, 23 and 24 to expose those areas of the gold conductor patterns 7, 8 and 9 where it is required to produce contact pips. (Figs. 5A, 5B). A coating 25 of an insulating lacquer, e.g. Bitulac (Registered Trade Mark) VB3106/70 manufactured by Bitulac Ltd, of Newcastle Upon Tyne is applied to the face of the slice opposite to that having the conductor patterns thereon.

3) Electrical contact is made to the chromium film 13, using a metal spring clip to contact this film directly, or indirectly by connecting the clip to the opposite face of the slice, a small area (about 1.5 mm square) of the photoresist or lacquer being removed from the array of transistor chips (not shown) for this purpose, and silver 11 is electroplated on to the gold conductors through the circular openings 22, 23 and 24 in the photoresist 21 to a height of about 25 μm (Figs. 6A, 6B). Well known silver cyanide electroplating solutions are used in which the array of transistor chips held in a Perspex (Registered Trade Mark) jig of known construction is immersed. The chromium film 13 serves to conduct electric current to the gold conductor pattern for the electroplating operation. It will be appreciated that the removal of the small area of photoresist 21 from the array causes the destruction of a few (e.g. about 4) individual transistor chips in the array. This can be avoided by causing the electroplating current to be applied through a small opening in the insulating lacquer on the under side of the array of transistor chips so that the current then reaches the chromium film 13 through the silicon slice 1, the collector contact regions 10 and aluminium layers 16.

4) The silver pips 11 are immediately electroplated with tin 12 to an additional height of 10 μm. Contact pips 4, 5 and 6 are thus produced comprising silver 11 and tin 12. (Figs. 6A, 6B).

5) The remaining photoresist is then removed and the exposed chromium film is etched away using a selective etchant, e.g. a solution of sodium hydroxide and potassium permanganate, which does not attack the gold conductor patterns 7, 8, 9 or the silver-tin pips 4, 5, 6. (Figs. 7A, 7B, 8).

The transistors are tested on a whole slice probing machine, faulty units are marked and the slice cut to produce individual transistor chips. The cutting up or dicing operation is carried out by well-known scribing or sawing techniques.

Transistor chips satisfying the electrical specification for the intended end use are cleaned and are then ready for mounting into a circuit. The transistors are bonded to conductors of thick or thin film circuits using the known solder flow technique.

It is not always essential to utilise con-

tact pips of a composite nature. For example, in the case where the conductors in the film circuit on which the transistors are to be mounted, is coated with soft solder, contact pips of a single solderable metal may be provided on the device.

Pips of other metals, e.g. nickel, lead, gold or copper can be formed by electroplating; these metals might be more suitable than silver for some applications. When thermocompression bonding techniques, well known in the art, are to be used for bonding the device to a circuit, gold is a suitable metal for the contact pips. Silver contact pips are also suitable when devices are to be connected to conductors in circuits by well-known ultrasonic bonding techniques. However, irrespective of the mounting technique used, an important requirement is that the contact pips should be sufficiently hard and have a sufficiently high melting point to maintain a space between the chip and the substrate during and after mounting. In this way a good contact is produced and electrical shorting between the electrodes and damage to the surface of the device is prevented.

As indicated above, one or more dummy pips may be plated to improve the mechanical stability of the assembly. Additionally, a number of transistors with some common terminals, each terminal having its own contact pip, can be produced on the same silicon chip which can then be mounted in the manner described. Diodes can be produced by a similar technique or complete circuits can be diffused into the chip by conventional monolithic techniques and terminal connections provided as described in the invention. Such complete integrated circuits can then be mounted on to a substrate in the manner described.

A method and apparatus for bonding small electronic components, e.g. devices of the type described, to conductor areas or lands on substrates, e.g. thick or thin film circuit elements, is described and claimed in our co-pending No. 11941/69 (Serial No. 1,250,847).

WHAT WE CLAIM IS:—

1. A silicon semiconductor device with diffused impurities therein forming diffused regions and provided with an apertured insulating film comprising a layer of silicon dioxide, which device is characterized by a metallic contact structure adapted to enable said device to be directly mounted on and electrically connected to a thick or thin film electrical circuit, said contact structure comprising a plurality of electrically conductive pips projecting from that surface of the device in which the diffused regions are situate and each of which is electrically linked with an associated diffused region through electrically conductive material in the apertures in the insulating film via an electrically conductive film composed of a chromium layer which is firmly adherent to said insulating film merging into a gold layer, said conductive pips being (i) of a height which is sufficient to provide clearance between the surface of the device on which they are situate and the circuit when the device is electrically connected and mounted thereon and (ii) composed of a material or combination of materials adapted to be electrically connected to a thick or thin film electrical conductor element by solder flow or ultrasonic or thermocompression bonding techniques, said chromium layer having sufficient electrical conductivity to carry electric current to allow the formation of said pips by electroplating and said gold layer having an electrical conductivity sufficient to carry an operating current for which the device is designed.

2. A device according to Claim 1, in which said chromium layer has a thickness of from 50 mμm to 400 mμm and said gold layer has a thickness of from 300 mμm to 2 μm.

3. A device according to Claim 1 or 2, in which, in addition to the said conductive pips, there is provided a further pip which is not electrically linked with the diffused regions, whereby stability is increased when the device is mounted on and electrically connected to the thick or thin film circuit.

4. A device according to Claim 1, 2 or 3, in which the conductive pips have a height of at least 10 μm.

5. A device according to Claim 4, in which said height is at least 25 μm.

6. A device according to any one of the preceding Claims, in which the conductive pips are of silver coated with a tin layer.

7. A silicon semiconductor device constructed and arranged substantially as herein described and shown in Figures 7A, 7B and 8 of the accompanying drawings.

8. A process for the production of a silicon semiconductor device with diffused impurities therein forming diffused regions and having (a) an insulating film comprising a layer of silicon dioxide having apertures therein containing electrically conductive material in electrical contact with the diffused regions, and (b), firmly adhering to said insulating film, an electrically conductive film of a chromium layer merging into a gold layer, the chromium layer being nearest to the insulating film, having good adhesion thereto and having sufficient electrical conductivity to allow electroplating by current passing through it, the gold layer having an electrical conductivity sufficient

to carry an operating current for which the device is designed, which process comprises

(i) selectively etching away part of said gold layer to expose the underlying chromium layer and to leave a pattern in said gold layer to provide electrical conductors extending from the electrically conductive material in contact with said diffused regions to areas where contact pips are to be produced,

(ii) coating the face of the device having the electrically conductive film thereon with a photoresist material and removing part of it to expose said areas,

(iii) masking the face opposite to that mentioned at (ii) against an electroplating solution,

(iv) electroplating metallic contact pips on said areas to a height which is sufficient to provide clearance between the surface of the device on which they are situate and the surface of a thick or thin film electrical conductor element when the device is electrically connected and mounted thereon, said pips being composed of a material or combination of materials adapted to be electrically connected to said element by solder flow or ultrasonic or thermocompression bonding techniques, the electroplating of the metallic contact pips being effected by using said chromium layer to carry the electroplating current to the areas where the pips are to be produced, and

(v) removing the remainder of said photoresist layer and etching away the exposed regions of said chromium layer using a selective etchant which does not attack either said gold layer or the contact pips.

9. A process according to Claim 8, in which the metallic contact pips are electroplated to a height of 10 μm or more.

10. A process according to Claim 9, in which the metallic contact pips are electroplated to a height of 25 μm or more.

11. A process according to Claim 8 substantially as herein described by reference to the specific method of producing a silicon semiconductor transistor chip constructed and arranged substantially as shown in Figures 7A, 7B and 8 of the accompanying drawings.

12. A silicon semiconductor device produced by the process claimed in any one of Claims 8 to 11.

13. A method of mounting a semiconductor device as claimed in any one of Claims 1 to 7 and 12 to a thick or thin film electrical circuit, which comprises the steps of positioning the semiconductor device with each conductive pip adjacent to a selected point on the electrical circuit path of the thick or thin film circuit and by solder flow or ultrasonic bonding or thermocompression bonding technique, or combinations of these, causing each conductive pip to become directly electrically connected to the circuit path to which it is adjacent, so as to form a secure electrical connection between the raised conductive pip and said circuit path, the solder flow or ultrasonic or thermocompression bonding being carried out in such a way that the semiconductor device remains spaced from the thick or thin film circuit after the completion of these operations.

14. A method according to Claim 13 substantially as herein described by reference to the transistor chip shown in Figures 7A, 7B and 8 of the accompanying drawings.

15. A thick or thin film electrical circuit having mounted thereon a semiconductor device produced by the process claimed in Claim 13 or 14.

for the Applicants:—

G. H. MUNSTER & CO.,
Chartered Patent Agents,
Imperial Buildings,
56 Kingsway,
London, W.C.2.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed. 1972.
Published at the Patent Office, 25 Southampton Buildings, London WC2A 1AY from which copies may be obtained.

1,288,564
2 SHEETS

COMPLETE SPECIFICATION

This drawing is a reproduction of the Original on a reduced scale.

SHEET 1

FIG. 1A.

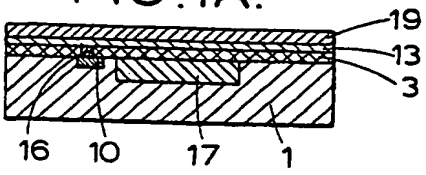

FIG. 1B.

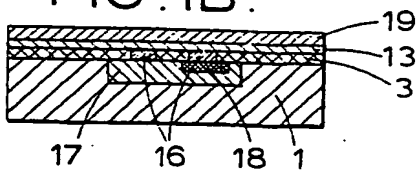

FIG. 2A.

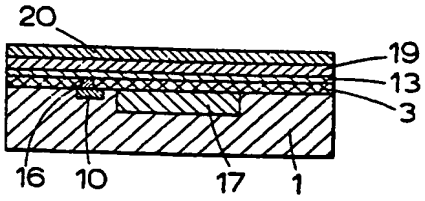

FIG. 2B.

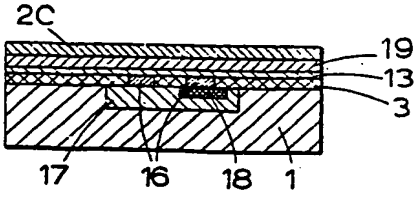

FIG. 3A.

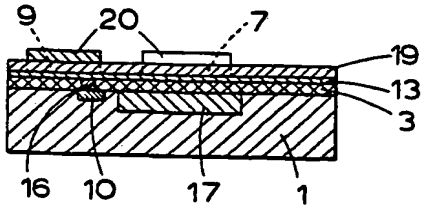

FIG. 3B.

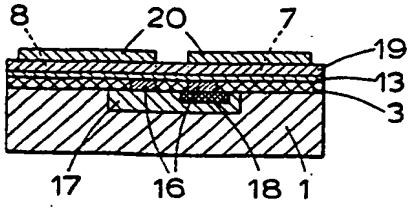

FIG. 1C.

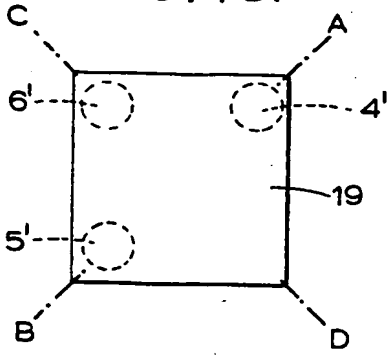

FIG. 3C.

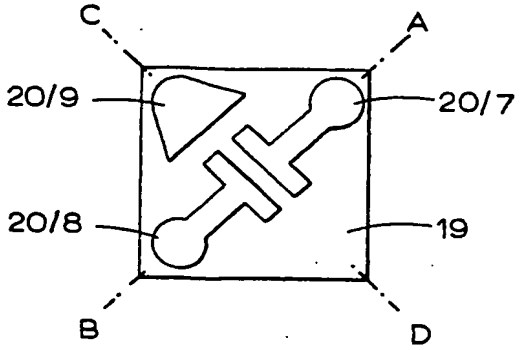

FIG.4A.

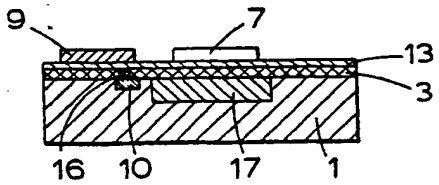

FIG.4B.

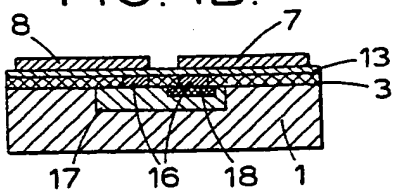

FIG.5A.

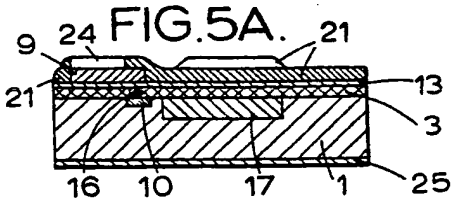

FIG.5B.

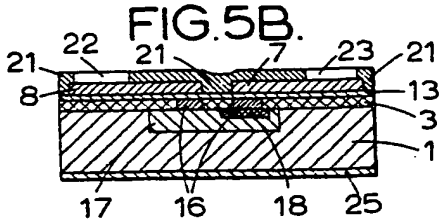

FIG.6A.

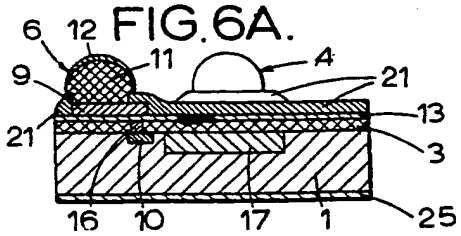

FIG.6B.

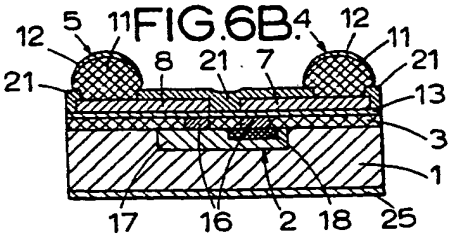

FIG. 7A.

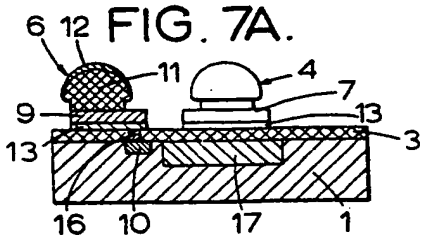

FIG. 7B.

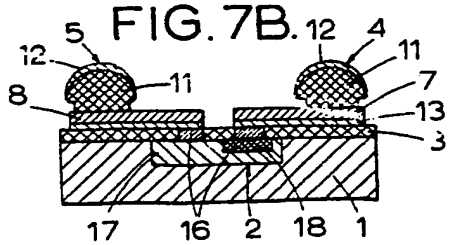

FIG. 8.

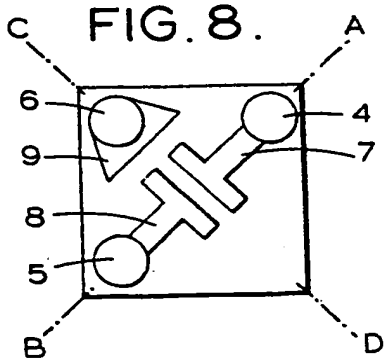

FIG.9.